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EXAMINER	
CRAWFORD, JASON	
ART UNIT	**PAPER NUMBER**
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/978,495	TOMSIO ET AL.	
	Examiner	Art Unit	
	Jason Crawford	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-51 and 53-58* is/are rejected.

7)☒ Claim(s) *52, 59-66* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/16/01
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-51 and 53-58 are rejected under 35 U.S.C. 102(b) as being anticipated by Yizraeli (US 5362996).

In regards to Claim 1, Yizraeli discloses of a method of transmitting signals in a network comprising of receiving a first (20, D0) and second (21, D1) adjacent signals, sensing simultaneous transition of the first (20) and second (21) signals (via 15), delaying the first signal (20) for a time period (via 30) and switching the second signal (21) and switching the first signal (20) after the time period. (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claims 2, 4, 7 and 9, Yizraeli discloses of the sensing being performed by a sensing (15) and delay (30-37) circuits. (Fig 1, Column 3 Lines 21-27)

In regards to Claim 3, Yizraeli discloses of the first signal (20) being delayed by a first buffer (40) and the second signal (21) being delayed by a second buffer (41) before switching. (Fig 1)

In regards to Claim 5, Yizraeli discloses of the sensing circuit (15) and delay circuits (30) provide a delay signal (14) to the first buffer (40) and delays the first signal

(20) until the second signal (21) switches (inherent since no two buffers are to be activated at one time, Column 1 Lines 66-67, Column 2 Line 1). (Fig 1)

In regards to Claim 6, Yizraeli discloses of receiving a third signal (22, D2) that is adjacent to the first (20) and second (21) signals and the method further comprising of sensing simultaneous transition of the third (22) and first (20) signals (via 15), delaying the first signal (20) for a time period (via 30), switching the third signal (22) and switching the first signal (20) after the time period. (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 8, Yizraeli discloses of the first signal (20) being delayed by a first buffer (40) before switching, the second signal (21) being delayed by a second buffer (41) before switching, and the third signal (22) being delayed by a third buffer (42) before switching. (Fig 1)

In regards to Claim 10, Yizraeli discloses of the sensing (15) and delay (30) circuits provide a delay signal (14) to the first buffer (40) to delay the first signal (20) until after the second (21) and third (22) signals are switched. (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 11, Yizraeli discloses of a method of transmitting signals in a network comprising of receiving a first (20, D0), second (21, D1), third (22, D2), fourth (23, D3) and fifth (24, D4) adjacent signals, sensing simultaneous transition of the first (20), second (21), third (22), fourth (23) and fifth (24) signals (via 15), delaying the first signal (20) when the second (21) has the same transition, delaying the third signal (22) in the event the second (21) and fourth (23) signals have the same transition as the

third signal (22) and delaying the fifth signal (24) in the event the fourth signal (23) transitions at the same time as the fifth signal (24). (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claims 12 and 14, Yizraeli discloses of the sensing being performed by a sensing (15) and delay (30-37) circuits. (Fig 1, Column 3 Lines 21-27)

In regards to Claim 13, Yizraeli discloses of the first signal (20) being delayed by a first buffer (40) before switching, the second signal (21) being delayed by a second buffer (41) before switching, the third signal (22) being delayed by a third buffer (42) before switching, the fourth signal (23) being delayed by a fourth buffer (43) before switching and the fifth signal (24) being delayed by a fifth buffer (44) before switching. (Fig 1)

In regards to Claim 15, Yizraeli discloses of the sensing (15) and delay circuit (30) providing a delay signal (14) to the first buffer (40) and delays the first signal (20) until the second signal (21) switches, the sensing (15) and delay circuit (32) providing a delay signal (14) to the third buffer (42) and delays the third signal (22) until the second (21) and fourth (23) signals switch, the sensing (15) and delay circuit (34) providing a delay signal (14) to the fifth buffer (44) and delays the fifth signal (24) until the fourth signal (23) switches (inherent since no two buffers are to be activated at one time, Column 1 Lines 66-67, Column 2 Line 1). (Fig 1)

In regards to Claim 17, Yizraeli discloses of a signal transmitting network comprised of a first device configured to receive first (20) and second (21) adjacent signals, delaying the first signal (via 30) for a time period, switching the second signal

(21) then switching the first signal (20) after the time period and a second device configured to sense simultaneous transitions (via 15) of the first (20) and second (21) signals (inherent since no two buffers are to be activated at one time, Column 1 Lines 66-67, Column 2 Line 1). (Fig 1)

In regards to Claim 16, Yizraeli discloses of a signal transmitting network comprised of a device to receive first (20) and second (21) adjacent signals, sense simultaneous transitions (via 15) of the first (20) and second (21) signals, delaying the first signal (via 30) for a time period, switching the second signal (21) then switching the first signal (20) after the time period (inherent since no two buffers are to be activated at one time, Column 1 Lines 66-67, Column 2 Line 1). (Fig 1)

In regards to Claim 18, Yizraeli discloses of the first signal (20) being delayed by a first buffer (40) and the second signal (21) being delayed by a second buffer (41) before switching. (Fig 1)

In regards to Claim 19, Yizraeli discloses of the sensing being performed by a sensing (15) and delay (30-37) circuits. (Fig 1, Column 3 Lines 21-27)

In regards to Claim 20, Yizraeli discloses of the second device (15) providing a delay signal (14) to the first buffer (40) and delays the first signal (20) until the second signal (21) switches. (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 21, Yizraeli discloses of receiving a third signal (22) adjacent to the first (20) and second (21) signals wherein the device is further configured to sense simultaneous transitions (via 15) of the third (22) and first (20) signals, delay the first signal (20) for a time period (via 30), switch the third signal (22) then switching the

first signal (20) after the time period. (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 22, Yizraeli discloses of a transmitting network comprised of a first device configure to receive first (20), second (21) and third (22) adjacent signals, delay the first signal (20) for a time period (via 30) and switch the third (22) signal, then the first (20) signal after the period of time and a second device configured to sense simultaneous transitions of the first (20) and third (22) signals (via 15) (inherent since no two buffers are to be activated at one time, Column 1 Lines 66-67, Column 2 Line 1). (Fig 1)

In regards to Claim 23, Yizraeli discloses of the first signal (20) being delayed by a first buffer (40) before switching, the second signal (21) being delayed by a second buffer (41) before switching, and the third signal (22) being delayed by a third buffer (42) before switching. (Fig 1)

In regards to Claim 24, Yizraeli discloses of the sensing being performed by a sensing (15) and delay (30-37) circuits. (Fig 1, Column 3 Lines 21-27)

In regards to Claim 25, Yizraeli discloses of the second device (15) providing a delay signal (14) to the first buffer (40) and delays the first signal (20) until the second (21) and third (22) signals switch. (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 27, Yizraeli discloses of a signal transmitting network comprised of a first device configure to receive first (20), second (21), third (22), fourth (23) and fifth (24) adjacent signals, delaying the first signal (20) in the event that the

second signal (21) transitions at the same time as the first signal (20), delaying the third signal (22) in the event that the second (21) and fourth (23) signals transition at the same time as the third signal (22), delaying the fifth signal (24) in the event that the fourth signal (23) transitions at the same time as the fifth signal (24) and a second device configured to sense simultaneous transitions (via 15) of the first (20), second (21), third (22), fourth (23) and fifth (24) signals (inherent since no two buffers are to be activated at one time, Column 1 Lines 66-67, Column 2 Line 1). (Fig 1)

In regards to Claim 26, Yizraeli discloses of a signal transmitting network comprised of a device configured to receive a first (20), second (21), third (22), fourth (23) and fifth (24) adjacent signal, sense simultaneous transitions (via 15) of the first (20), second (21), third (22), fourth (23) and fifth (24) signals, delaying the first signal (20) in the event that the second signal (21) transitions at the same time as the first signal (20), delaying the third signal (22) in the event that the second (21) and fourth (23) signals transition at the same time as the third signal (22), and delaying the fifth signal (24) in the event that the fourth signal (23) transitions at the same time as the fifth signal (24) (inherent since no two buffers are to be activated at one time, Column 1 Lines 66-67, Column 2 Line 1). (Fig 1)

In regards to Claim 28, Yizraeli discloses of the first signal (20) being delayed by a first buffer (40) before switching, the second signal (21) being delayed by a second buffer (41) before switching, the third signal (22) being delayed by a third buffer (42) before switching, the fourth signal (23) being delayed by a fourth buffer (43) before

switching and the fifth signal (24) being delayed by a fifth buffer (44) before switching. (Fig 1)

In regards to Claim 29, Yizraeli discloses of the sensing being performed by a sensing (15) and delay (30-37) circuits. (Fig 1, Column 3 Lines 21-27)

In regards to Claim 30, Yizraeli discloses of the sensing (15) and delay circuit (30) providing a delay signal (14) to the first buffer (40) and delays the first signal (20) until the second signal (21) switches, the sensing (15) and delay circuit (32) providing a delay signal (14) to the third buffer (42) and delays the third signal (22) until the second (21) and fourth (23) signals switch, the sensing (15) and delay circuit (34) providing a delay signal (14) to the fifth buffer (44) and delays the fifth signal (24) until the fourth signal (23) switches(inherent since no two buffers are to be activated at one time, Column 1 Lines 66-67, Column 2 Line 1). (Fig 1)

In regards to Claim 31, Yizraeli discloses of an apparatus for transmitting signals in a network comprised of means for receiving first (20) and second (21) adjacent signals, means for sensing simultaneous transitions (via 15) of the first (20) and second (21) signals, means for delaying the first signal (via 30) for a time period, means for switching the second signal (21), and means for switching the first signal (20) after the time period. (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claims 32, 34, 37 and 39, Yizraeli discloses of the means for sensing being performed by a sensing (15) and delay (30-37) circuits. (Fig 1, Column 3 Lines 21-27)

In regards to Claim 33, Yizraeli discloses of the first signal (20) being delayed by a first buffer (40) and the second signal (21) being delayed by a second buffer (41) before switching. (Fig 1)

In regards to Claim 35, Yizraeli discloses of sensing (15) and delay (30) circuits providing a delay signal (14) to the first buffer (40) and delays the first signal (20) until the second signal (21) switches. (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 36, Yizraeli discloses of means for receiving a third signal (22) adjacent to the first (20) and second (21) signals, means for sense simultaneous transitions (via 15) of the third (22) and first (20) signals, means for delay the first signal (20) for a time period (via 30), means for switching the third signal (22), and means for switching the first signal (20) after the time period. (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 38, Yizraeli discloses of the first signal (20) being delayed by a first buffer (40) before switching, the second signal (21) being delayed by a second buffer (41) before switching, and the third signal (22) being delayed by a third buffer (42) before switching. (Fig 1)

In regards to Claim 40, Yizraeli discloses of the sensing (15) and delay (30) circuits providing a delay signal (14) to the first buffer (40) and delays the first signal (20) until the second (21) and third (22) signals switch. (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 41, Yizraeli discloses of an apparatus for transmitting signals in a network comprised of means for receiving first (20), second (21), third (22), fourth

(23) and fifth (24) adjacent signals, means for sensing simultaneous transitions (via 15) of the first (20), second (21), third (22), fourth (23) and fifth (24) signals, means for delaying the first signal (via 30) in the event the second signal (21) transitions at the same time as the first signal (20), means for delaying the third signal (22) in the even the second (21) and fourth (23) signals transition at the same time as the third signal (22) and means for delaying the fifth signal (24) in the even the fourth signal (23) transitions at the same time as the fifth signal (24). (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claims 42 and 44, Yizraeli discloses of the means for sensing being performed by a sensing (15) and delay (30-37) circuits. (Fig 1, Column 3 Lines 21-27)

In regards to Claim 43, Yizraeli discloses of the first signal (20) being delayed by a first buffer (40) before switching, the second signal (21) being delayed by a second buffer (41) before switching, the third signal (22) being delayed by a third buffer (42) before switching, the fourth signal (23) being delayed by a fourth buffer (43) before switching and the fifth signal (24) being delayed by a fifth buffer (44) before switching. (Fig 1)

In regards to Claim 45, Yizraeli discloses of the sensing (15) and delay (30) circuits providing a delay signal (14) to the first buffer (40) and delays the first signal (20) until the second (21) signal switches, the sensing (15) and delay (32) circuit provides a delay signal (14) to the third buffer (42) to delay the third signal (22) until the second (21) and fourth (23) signals switch and the sensing (15) and delay (34) circuit

provides a delay signal (14) to the fifth buffer (44) to delay the fifth signal (24) until the fourth signal (23) switches. (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 46, Yizraeli discloses of an apparatus comprised of a circuit (15) configured to detect a transition of first (20) and a second (21) signals and provide a delay signal (14) when the transitions of the first (20) and second (21) signals occur simultaneously and a first buffer (40) coupled to the circuit wherein the first buffer (40) is configured to delay the transition of the first signal (20) in response to the delay signal (14). (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 47, Yizraeli discloses of the first buffer (40) being configured to delay the transition of the first signal (20) until the transition of the second signal (21) has completed (inherent since no two buffers are to be activated at one time, Column 1 Lines 66-67, Column 2 Line 1). (Fig 1)

In regards to Claim 48, Yizraeli discloses of the circuit (15) is further configured to detect the transition of a third signal (22) and provide a delay signal (14) when the transition of the first (20) and third (22) signals occur simultaneously (inherent since no two buffers are to be activated at one time, Column 1 Lines 66-67, Column 2 Line 1). (Fig 1)

In regards to Claim 49, Yizraeli discloses of the first buffer (40) being configured to delay the transition of the first signal (20) until the transition of the third signal (22) has completed (inherent since no two buffers are to be activated at one time, Column 1 Lines 66-67, Column 2 Line 1). (Fig 1)

In regards to Claim 50, Yizraeli discloses of a second buffer (41) to receive a second signal (21) and provide a delayed second signal (Q1) wherein the delay of the second buffer (41) is inherently equal to the delay of the first buffer (40) and Yizraeli also discloses of a third buffer (42) configured to receive a third signal (22) and provide a delayed third signal (Q2) wherein the delay of the third buffer is inherently equal to the delay of the first buffer (40). (Fig 1)

In regards to Claim 51, Yizraeli discloses of the first (20), second (21) and third (22) signals are adjacent. (Inherent in Fig 1)

In regards to Claim 53, Yizraeli discloses of the apparatus being coupled to an integrated circuit. (Column 1 Lines 58-60)

In regards to Claim 54, Yizraeli discloses of an apparatus comprising a circuit (15) configured to detect a transition of a plurality of signals (20-27) and provide a delay signal (14) when any adjacent signals simultaneously transition and a plurality of buffers (40-47) coupled to the circuit (15) wherein at least one buffer of the plurality is configured to delay at least one transition in response to the delay signal (14). (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 55, Yizraeli discloses of the apparatus of Claim 54 wherein at least one buffer (40-47) is configured to delay at least one transition until all other adjacent transitions have completed. (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 56, Yizraeli discloses of a first circuit (15) configured to detect the transition of a first signal (20) and a second signal (21) and provide a first delay

signal (14) when the transitions of the first (20) and second (21) signals occur simultaneously, and a first buffer (40) coupled to the first circuit (15) wherein the first buffer (40) is configured to delay the transition of the first signal (20) in response to first delay signal (14). (Fig 1, Column 2 Lines 3-8 and Column 4 Lines 20-25)

In regards to Claim 57, Yizraeli discloses of the first signal (20) being adjacent to the second signal (21). (Inherent in Fig 1)

In regards to Claim 58, Yizraeli discloses of the first buffer (40) being configured to delay the transition of the first signal (20) until the transition of the second signal (21) has completed (inherent since no two buffers are to be activated at one time, Column 1 Lines 66-67, Column 2 Line 1). (Fig 1)

Allowable Subject Matter

Claims 52 and 59-66 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In regards to Claim 52, the prior art does not directly disclose of the apparatus of Claim 50 further comprising a first sense signal wherein the first signal is coupled to the circuit via the first sense signal, a second sense signal wherein the second signal is coupled to the circuit via the second sense signal and a third sense signal wherein the

third signal is coupled to the circuit via the third sense signal, nor would it have been obvious to one of ordinary skill in the art to do so.

In regards to Claim 59, the prior art does not directly disclose of the apparatus of Claim 56 further comprising a second circuit configured to detect a transition of the second signal, third signal and fourth signal and provide a second delay signal when the transition of the third occurs simultaneously with at least one of the transitions of the second signal and the fourth signal and a second buffer coupled to the second circuit wherein the second buffer is configured to delay the transition of the second signal in response to the second delay signal, nor would it have been obvious to one of ordinary skill in the art to do so. Therefore, Claims 60-65 are also objected to as being dependent on the objected Claim 59.

In regards to Claim 66, the prior art does not directly disclose of the apparatus of Claim 54 further comprising a second circuit configured to detect a transition of each signal of a second plurality of signals and provide a second delay signal when any adjacent signals simultaneously transition, nor would it have been obvious to one of ordinary skill in the art to do so.

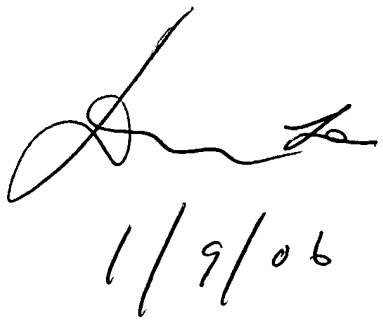
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Crawford whose telephone number is 571-272-6004. The examiner can normally be reached on Monday - Friday 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rex Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMC



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DON LE
PRIMARY EXAMINER